TITLE

GATE OXIDE MEASUREMENT APPARATUS

BACKGROUND OF THE INVENTION

Field of the Invention

The invention relates to a measuring apparatus, and more particularly to an apparatus for measuring the thickness of a gate oxide layer of a vertical transistor and a gate oxide thickness measurement.

Description of the Related Art

With the wide application of integrated circuits (ICs), several kinds of semiconductor devices with higher efficiency and lower cost are produced based on different objectives. The dynamic random access memory (DRAM) is an important semiconductor device in the information and electronics industry. Basically, a DRAM is an integrated circuit that stores data in binary form (e.g., "1" or "0") in a large number of cells.

Most DRAMs have one transistor and one capacitor in one DRAM cell. The memory capacity of the DRAM has reached 256 megabits. Therefore, integration increases size of the memory cell and the transistor must be reduced yield DRAM with higher memory capacity and higher processing speed. A 3-D capacitor structure can reduce the area occupied by memory cells on the semiconductor substrate. Accordingly 3-D capacitors, such as a deep trench capacitors, are applied in the fabrication of the DRAM with capacity of 64 megabits or greater. A conventional DRAM module with a plane transistor covers a larger area of the semiconductor substrate surface and cannot satisfy

high integration requirements. Therefore, space saving vertical transistors have become a trend in memory cell fabrication.

However, in vertical transistors, the break down voltage of a gate oxide layer suffers when the width of the active area is altered. Conventional techniques do not provide a method or an apparatus to measure thickness of the gate oxide layer of the vertical transistor.

SUMMARY OF THE INVENTION

The present invention is directed to estimating a thickness of a gate oxide layer.

Accordingly, the present invention provides a apparatus for measuring a gate oxide layer disposed in a scribe line region, comprising, a first active area disposed on a substrate, a first active area with a predetermined width with of at least 2F, first to fifth wordlines disposed on the substrate in a first direction with a first predetermined space between each two wordlines, and the first ends of the first to fifth wordlines are electrically connected. First and second bar-shaped trench capacitors are disposed under the second and the fourth wordlines respectively, with a second predetermined space between the first and second bar-shaped trench capacitors, the first and second bar-shaped trench capacitors are longer than the first active area; wherein the first space is smaller than the second space, and F is a minimum line width of the wordlines; and first and second gate structures are respectively disposed between the first bar-shaped trench capacitor and the second wordline and between the second bar-shaped trench capacitor and the fourth wordline, each gate

structure comprising a gate conducting layer and a gate oxide layer, wherein the gate conducting layers are electrically connected to the wordlines respectively.

The present invention also provides a gate oxide thickness measurement. A wafer with a scribe line and a memory cell area is provided. A measuring apparatus is formed on the scribe line, and a plurality of memory cells with vertical transistors is formed in the memory cell area, and each vertical transistor has a gate oxide layer. The measuring apparatus comprises a first active area, first to fifth wordlines, first and second bar-shaped trench capacitors, and first and second gate structures. The first active area is disposed on a substrate, and has a predetermined width of at least 2F. The first to fifth wordlines are disposed on the substrate in a first direction, with a minimum line width of F between each two wordlines, and the first ends of the first to fifth wordlines are electrically connected. The first and second bar-shaped trench capacitors are disposed under the second and fourth wordlines respectively and are longer than the first active area, a predetermined space of 3F between exists between the first and second bar-shaped trench capacitors. The first and second gate structures are respectively disposed between the first bar-shaped trench capacitor and the second wordline and between the second bar-shaped trench capacitor and the fourth wordline, each gate structure comprising a gate conducting layer and a gate oxide layer, wherein the gate conducting layers are electrically connected to the wordlines respectively. An equivalent capacitance between the first conducting and the first active area is measured. Thickness of the gate oxide layer of the measuring apparatus is estimated according to

the equivalent capacitance. The gate oxide layer thickness of each vertical transistor is estimated according to the thickness of the gate oxide layer of the measuring apparatus.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, reference is made to a detailed description to be read in conjunction with the accompanying drawings, in which:

FIG. 1 shows a layout of a memory cell in a memory cell area of the present invention;

FIG. 2 is a cross-section of the memory cell of the present invention;

FIG. 3 shows a layout of a measuring apparatus of the present invention;

FIG. 4 is a cross-section of the measuring apparatus of the present invention;

FIGs. 5a and 5b are equivalent circuit diagrams of the capacitor of the present invention;

FIG. 6 shows another layout of the measuring apparatus of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

The present invention provides an apparatus for measuring a thickness of a gate oxide layer of a vertical transistor and a gate oxide thickness measurement.

FIG. 1 shows a layout of a memory cell in a memory cell area of the present invention, FIG. 2 is a cross-section of the memory cell of the present invention, and FIG. 3 shows the layout of a measuring apparatus of the present invention. A wafer is first provided. A plurality of memory cells is formed

on a memory cell area 100 of the wafer, and a measuring apparatus 200 is formed on the scribe line region of the wafer.

In FIGS. 1 and 2, a plurality of trench capacitors is disposed on a substrate of the memory cell area 100, and the adjacent trench capacitors 10 are arranged in a separation region. A plurality of active areas 14 is disposed on the substrate in a horizontal direction, and each active area 14 is formed above each trench 10. A plurality of wordlines 12 is disposed on the substrate in a perpendicular direction. A gate structure GC is disposed between each wordline 12 and the trench capacitor 10 thereunder. The conducting layer 16, an insulating layer GOX, and a doping area 18 respectively act as a gate, a gate oxide layer, and a source of a vertical transistor. The doping area 18 is electrically connected to a corresponding trench capacitor 10.

In FIGs. 3 and 4, in the measuring apparatus 200 of the present invention, a first active area 141 is disposed on a substrate, and a width of the first active area 141 is a predetermined width of at least 2F. Wordlines 121 are disposed on the substrate in a first direction, with a minimum line width F between each two wordlines, each wordline has a first end, and the first ends are electrically connected. In the embodiment, the first ends of the wordlines 121 are electrically connected by a first conducting layer 201. Bar-shaped trench capacitors 101 are disposed on the substrate, with a predetermined space of about 3F between each two bar-shaped trench capacitors 101. A first trench capacitor 101 and a second trench capacitor 101 are longer than the first active area 141. The wordlines 121 are disposed above the corresponding bar-shaped trench capacitors 101, and

electrically connected to the corresponding bar-shaped trench capacitors 101. The gate structures GC are disposed between the bar-shaped trench capacitor 101 and the wordlines 121, each gate structure GC includes a gate conducting layer 161 and a gate oxide layer GOX, and each gate conducting layer 161 is electrically connected to the corresponding wordline 121. A doped layer 22 is disposed on the substrate under a second end of each wordline 121.

Hereinafter, the method for forming the structures of the present invention is described.

In the embodiment, when the trench capacitors 10 (in FIG. 1 and FIG. 2) of the memory cell are formed on the memory cell area of the wafer, the bar-shaped trench capacitors 101 are formed on the scribe line region of the wafer using the same mask and process parameters at the same time. The width of the trench capacitor 101 is 1F, and the space between each two trench capacitors 101 is 3F, wherein F is a minimum line width of one wordline.

Afterward, when the active areas 14 on the memory cell area are defined, the active areas 141 are defined on the scribe line region of the wafer at the same time using the same mask and process parameters. The width of each active area 141 is 2F, and each active area 141 is approximately perpendicular to each bar-shaped trench capacitor 101.

Thereafter, when the gate structures GC are formed on the memory cell area 100, gate structures GC1 are formed above the corresponding bar-shaped trench capacitors 101 at the same time using the same mask and process parameters. Each gate structure GC1 has a gate conducting layer 161 and a gate oxide layer GOX.

When the wordlines 12 of the memory cells on the memory cell area 100 are formed, wordlines 121 are formed in the active areas 141 on the scribe line at the same time using the same mask and process parameters. The wordlines 121 are disposed in parallel on the scribe line, and the space between each two wordlines 121 is a minimum line width F. Further, each gate structure GC1 is electrically connected to the corresponding wordline formed thereon.

Hereinafter, the method for measuring the thickness of the gate oxide is described.

An equivalent capacitance between the first conducting layer 121 and the active area 141 is measured. A thickness of the gate oxide layer GOX of the measuring apparatus is estimated according to the equivalent capacitance. In the embodiment, a capacitor C_{GOX} structure comprises the active area 141, the wordline 121, and the gate oxide layer GOX.

For example, the active area 141 acts as an upper plate, the gate oxide GOX acts as an insulating layer of the capacitor C_{GOX}, and the wordline 121 acts as a bottom plate of the capacitor C_{GOX}. Therefore, an equivalent capacitance C_S is measured between the wordline 121 and the active area 141, and the equivalent capacitance C_S is connected in parallel to the capacitors C_{GOX} in FIGs. 5a and 5b.

The thickness d of the gate oxide layer GOX of the measuring apparatus is obtained according to the formula: $C=\frac{\varepsilon}{d}\times A$, wherein C is the equivalent capacitance C_S, ε is a dielectric constant of the gate oxide layer GOX, and A is a contact area between the gate oxide layer GOX of the measuring apparatus and the active area 141. Therefore, the thickness of the gate

oxide layer GOX of the measuring apparatus may be obtained according to the capacitance C_S of the present invention.

The gate structures GC on the memory cell area and the gate structures GC1 on the scribe line are formed using the same masks and the process parameters, and thus the gate oxide layer GOX of the vertical transistor on the memory cell area is obtained according to the thickness of the gate oxide layer GOX of the measuring apparatus.

In the present invention, the structures on the scribe line region and the memory cell area are fabricated simultaneously to reduce fabrication time, hence, the thickness of the gate oxide layer of the vertical transistor can be estimated, and the measuring apparatus does not occupy space in the memory cell area.

In FIG. 6, the measuring apparatus of the present invention further comprises a second active area 142, and a width of the active area 142 is at least 2F. The second active area 142 is disposed on the substrate in a second direction with the first active area 141, and the first active area 141 is electrically connected to the second active area 142 by a second conducting layer 202. Similarly, the equivalent capacitance C_S is measured between the first conducting layer 121 and the active areas 141 and 142.

The capacitor C_{GOX} structure comprises the active areas 141 and 142, the wordline 121, and the gate oxide layer GOX. Therefore, the thickness of the gate oxide layer GOX of the measuring apparatus is obtained according to the formula: $C=\frac{\varepsilon}{d}\times A$, wherein C is the equivalent capacitance C_S, ε is a dielectric constant of the gate oxide layer GOX, and A is a

contact area between the gate oxide layer GOX of the measuring apparatus and the active areas 141 and 142. The gate structures GC on the memory cell area and the gate structures GC1 on the scribe lines are formed using the same masks and the process parameters, and thus the gate oxide layer GOX of the vertical transistor on the memory cell area is obtained according to the thickness of the gate oxide layer GOX of the measuring apparatus.

Similarly, the measuring apparatus and the measurement of the present invention can be executed by a plurality of active areas arranged in the horizontal direction, wherein the active areas are electrically connected with each other. That is, the active areas may be electrically connected with each other by a conducting layer.

While the invention has been described by way of example and in terms of the preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiments. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.